The 'Polly' Audio Store

Save your throat during the next contest - let Polly do the talking!

by Keith Orchard, G3TTC *

POLLY IS DESIGNED to store 60 seconds of audio, and has numerous applications, not the least of which is avoiding throat problems during phone contests! It affords easy recording and playback, and the 60 seconds total time is divisible into smaller segments if needed. It operates from a single 5-volt supply.

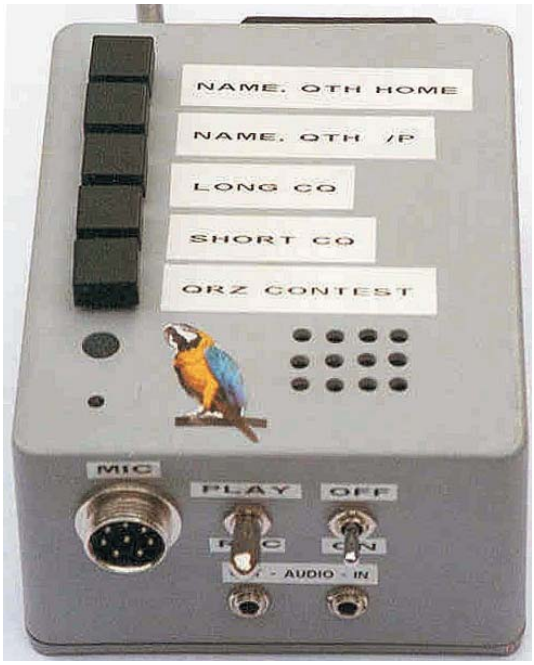
INTRODUCTION

THE HEART OF THE UNIT is an ISD2560 chip which records and plays back audio with a minimum of external circuitry. This particular chip has an audio bandwidth of 3.4kHz and a recording duration of 60 seconds.

Each chip has a microphone preamplifier, AGC, anti-aliasing and smoothing filters, a high-density multi-level storage array, speaker driver, control interface and an internal precision reference clock, see **Fig 1**.

The advantage of using an EEPROM (Electrically-Erasable Programmable Read-Only Memory) is that it is non-volatile, ie data are retained in the chip when power is removed. Other impressive claims by the manufacturer include 100-year message retention and 100,000 record cycles (typical figures).

* 32 Myton Crescent, Warwick CV34 6QA.



It never tires of talking: the Polly prototype.

The speech samples are stored directly into the on-chip non-volatile memory without the digitisation and compression associated with other methods of processing. Chips can be cascaded if required. The pin connections are described in the sidebar on p19 and illustrated in Fig 1.

DESCRIPTION

THE UNIT IS CONSTRUCTED in a small diecast box containing two PCBs. On board 1 are mounted the programming diodes, while board 2 has three ICs - IC1, IC2 and IC3. The circuits of the two PCBs are shown in **Fig 2** and **Fig 3**.

IC2 is used as a pulse-stretcher for the Overflow LED. The OVF output from IC1 is a 6.5µs pulse, which is stretched to 120ms, a value suitable for driving the LED. When on *Record*, the LED flashes when the memory is completely full; on *Playback*, the LED pulses once at the end of each recording. The NE556N is a dual timer, though only one half is used. It was originally intended to use the other half as another pulse stretcher, but in the end was not used. The NE556N could quite easily be replaced by an NE555N, an eight-pin DIL device, with appropriate changes to the connections.

The voltage regulator used for IC3 could be any 5V output device capable of supplying 50mA. The advantage of using the HT7250 device is that it will operate satisfactorily with its input as low as 5.1V.

D36 protects the ICs against reverse connection of the battery. RV1 allows the output audio level to be adjusted. The loudspeaker impedance can be 16 to 40Ω. R12 is used to adjust the volume to a suitable level. The minimum load impedance presented across pins 14 and 15, according to the ISD2560 specification, should be 16Ω. The *Audio In* jack is used where an external audio signal is

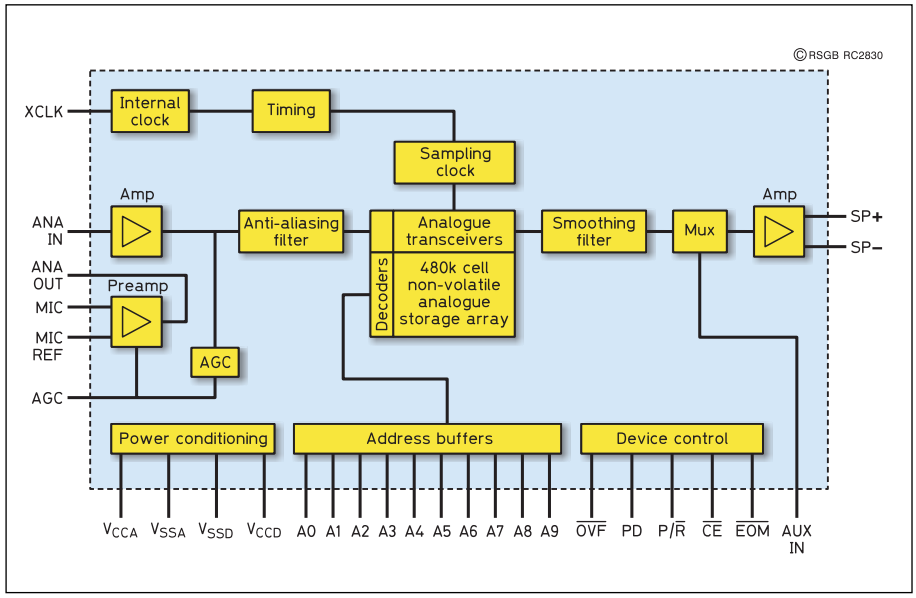


Fig 1: The ISD2560 block diagram.

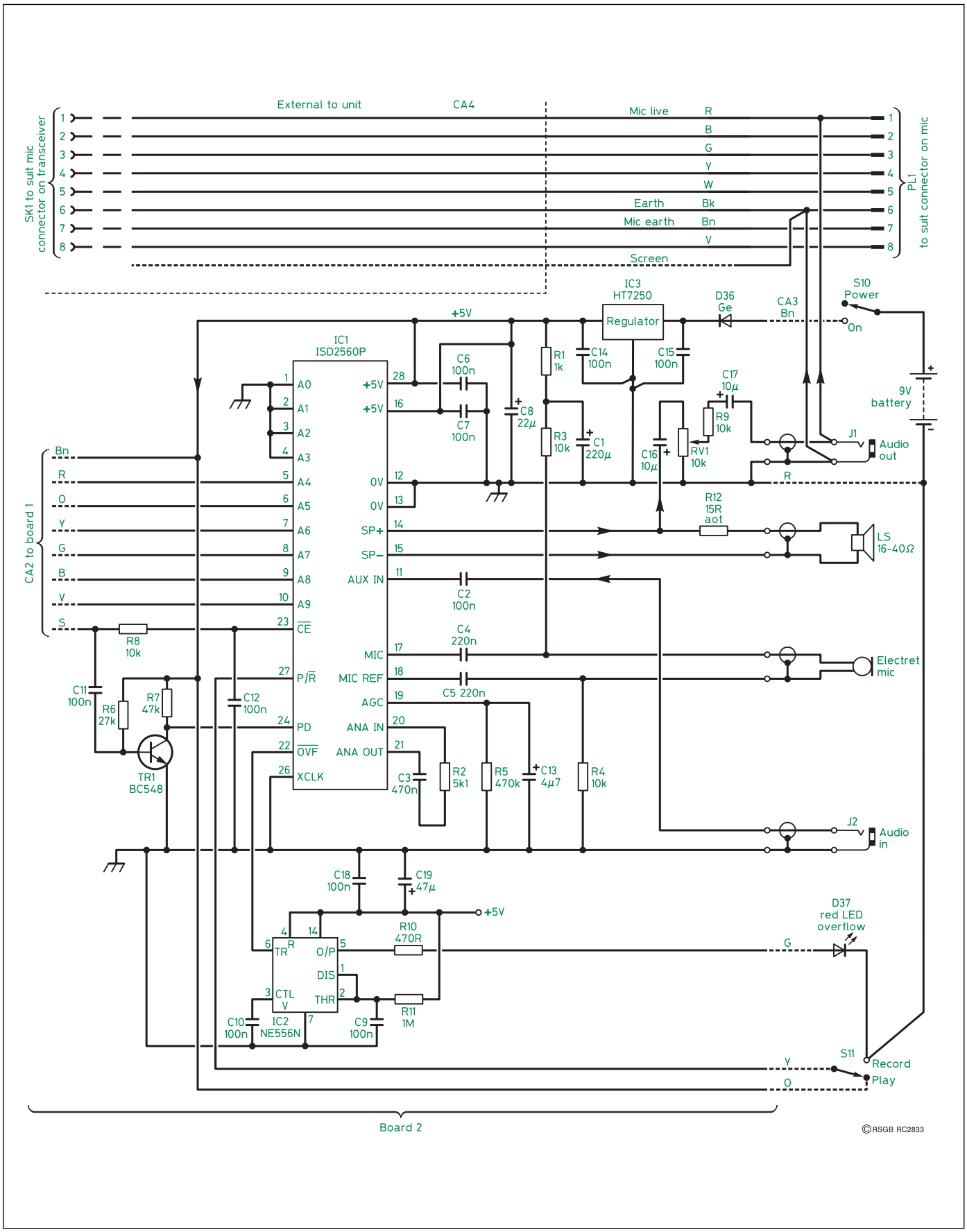


Fig 2: The circuit diagram of board 2.

PIN CONNECTIONS for the ISD2560P

- **Pins 1-10** carry memory address lines A0 to A9. These lines can access six hundred cells each of 0.1 second duration, totalling 60 seconds. However, in other applications, if address lines A8 and A9 are held high, representing an address of 768 (decimal), the remaining address signals are interpreted as mode bits instead of address bits. Further information on these operational modes can be found in the ISD Data Book [1].
- **Pin 11 (Auxiliary Input, AUX IN)** is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is high, P/R is high, and Playback is currently not active or if the device is in Playback Overflow. When cascading devices for longer durations, the speaker output from one device can feed the auxiliary input of the following device.
- **Pins 12 and 13 (Vssd and Vssa**) are the 0V supply rails for the digital and analogue circuits, respectively.
- **Pins 14 and 15 (Speaker Outputs, SP+ and SP-)** - a differential speaker driver output capable of dissipating 50mW in a 16Ω load.
- **Pin 16 (Vcca)** is the analogue positive supply pin, +4.5v to +5.5v.
- **Pins 17 and 18 (Microphone and Microphone Reference, MIC and MIC REF)** are two input pins. The mic input feeds an on-chip pre-amplifier with AGC producing a gain of –15 to +24dB. AC coupling should be used on both input pins, and the capacitor value used determines the low-frequency roll-off. The Mic Ref input is the inverting input to the microphone pre-ampifier, for use in conjunction with a differential microphone.
- **Pin 19 (AGC)**. The AGC dynamically adjusts the pre-amplifier gain for a wide range of microphone input levels, with minimal distortion. External components connected between this pin and earth determine the AGC attack and release time constants.
- **Pin 20 (Analogue In, ANA IN)**. See pin 21.
- **Pin 21 (Analogue Out, ANA OUT)** is the pre-ampifier output, normally connected via external components to the Analogue Input (pin 20) for recording. The value of the capacitor is selected to give additional LF roll-off.
- **Pin 22 (Overflow Output, $\overline{OVF}$)**. The signal on this pin pulses low when the last message has filled the memory and starts to overflow. As each pulse is only 6.5µs long, a pulse stretcher is required to drive an LED.
- **Pin 23 (Chip Enable Input, $\overline{CE}$)**. When this pin is taken low, the falling edge latches the address inputs and Playback/Record input P/$\overline{R}$.
- **Pin 24 (Power Down Input, PD)**. When not recording or playing back, this pin should be held high to place the device in the low consumption mode, 1µA typical.
- **Pin 25 (End-of-Message Output, $\overline{EOM}$)**. A marker is automatically inserted at the end of each message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses low for 12ms at the end of each message.
- **Pin 26 (External Clock Input, Xclk)**. When not required for precision applications, this pin is earthed.
- **Pin 27 (Playback/Record Input, P/$\overline{R}$)**. This input is latched by the falling edge of the $\overline{CE}$ pin. A high level selects a Playback cycle whereas a low selects a Record cycle. For a Playback cycle, the address inputs provide the starting address and the device will play until an EOM marker is encountered. For a Record cycle, the address inputs provide a starting address and recording continues until PD or $\overline{CE}$ is pulled high or an overflow is detected.
- **Pin 28 (Vccd)** is the digital positive supply pin, +4.5 to +5.5V.

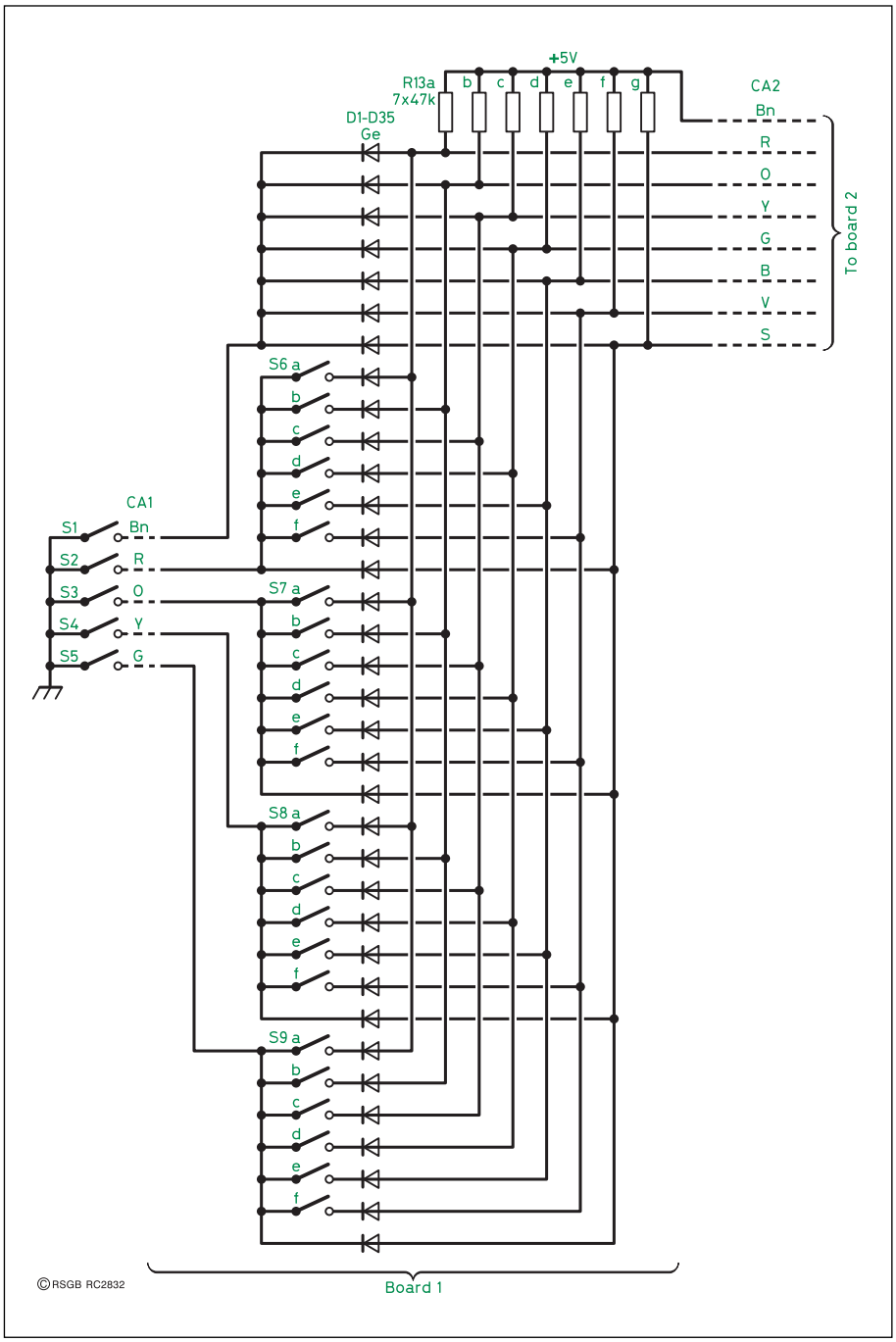


Fig 3: The circuit of board 1.

to be recorded. If the audio output is required to drive an amplifier, it can be taken from the *Audio Out* jack. As made, the unit is intended to be used with an IC-735 transceiver. It could, however, be wired using appropriate microphone connectors to suit other transceivers. Alternatively, the audio could just be available on the *Audio Out* jack for connecting to a transceiver. It would be necessary to wire a jack in parallel with the transceiver microphone connector to receive the audio, unless this connection is already accessible on another connector on the rear of the transceiver.

MEMORY

THE 60-SECOND total storage time of the device can be subdivided into a number of shorter periods, as desired, five periods seeming to be a reasonable figure.

There are 10 address lines, A0 to A9, see Figs 1 and 2. By grounding the four least significant lines, A0 to A3, this leaves six to be connected to addressing switches, giving a resolution of 1.6 seconds, which is quite adequate for most needs. This means that the recording lengths of the five periods can each be adjusted in 1.6-second increments.

The first recording period, initiated by S1, always starts at time 0 (zero) seconds. The second recording period, initiated by S2, starts at a time as set on the DIL switch S6a-f. Subsequent periods, initiated by S3, S4 and S5 start at times as set by the DIL switches S7a-f, S8a-f and S9a-f respectively. **Table 1** shows how the DIL switches should be set for particular start times.

COMPONENTS

Resistors (all 5%, 0.25W minimum)

R1	1k
R2	5k1
R3,4,8,9	10k
R5	470k
R6	27k
R7	47k
R10	470R
R11	1M
R12	15R Adjust on test (wired between Veropins)
R13a-g	7 x 47k SIL resistor array or use separate resistors. See text.
RV1	Preset potentiometer, side adjust, PCB vertical mounting, 10k

Capacitors

C1	220µF electrolytic
C2, 6, 7, 9, 10, 11, 12, 14, 15, 18	0.1µF
C3	0.47µF
C4,5	0.22µF
C8	22µF tantalum
C13	4.7µF tantalum
C16,17	10µF tantalum
C19	47µF

Semiconductors

IC1	ISD 2560P	NM52G
IC2	NE556N.	QH67X
IC3	5V 100mA regulator, general purpose, or use HT7250	LE79L
TR1	Silicon NPN general purpose transistor, BC548, 2N2222 or similar	
D1 – D36	Germanium diode, general purpose, OA47 or similar	
D37	Red LED, sub-miniature	

Miscellaneous

CA1	Cable, ribbon, multi-coloured, 5 way, 200mm long	XR06G
CA2	Cable, ribbon, multi-coloured, 8 way, 150mm long	XR06G
CA3	Cable, ribbon, multi-coloured, 5 way, 250mm long	XR06G
CA4	Cable, multi-core, 8 way, flexible, 400-600mm long	
J1, J2	3.5mm mono jack socket, panel mounting	
JS1-JS6	PCB jumper strip (optional) or wire links	
LS	16-40Ω loudspeaker, 50mm dia	
Mic	Ultra-miniature electret insert, both connections isolated from earth	QY62S
PL1	Locking 8-way plug, panel mounting, as required to suit mic	FK29G
SK1	Locking 8-way socket, cable mounting as required to suit transceiver	FK30H
S1 – S5	Miniature push-button switch, SPST, panel mounting	
S6 – S9	Miniature dual-in-line switch (6), SPST or SPDT, PCB mounting	
S10, S11	Miniature toggle switch, SPDT (S11 optional locking type)	
Board 1	Veroboard, 0.1in matrix, 95mm wide, track 76mm long. See text	
Board 2	Veroboard, 0.1in matrix, 95mm wide, track 86mm long. See text	
	Diecast aluminium box, 119 x 93 x 55mm or similar	
	PP3 battery and holder	
	Hardware: Screws, 5 and 12mm spacers, Veropins, single screened cable, etc	
	IC sockets: 28-pin and 14-pin.	

Maplin codes are given where specific components are useful in the construction.

CONSTRUCTION

THE PROTOTYPE WAS HOUSED in a 119mm long x 93mm wide x 55mm high diecast aluminium box, with very little spare space. Most components were mounted on two stacked pieces of Veroboard fixed to the lid of the box. On board 1 were mounted the programming diodes and dual-in-line switches, while the ISD2560P, NE556N and the remaining components were on board 2. The two boards were interconnected by a ribbon cable. Board 2 was mounted closest to the lid because access was not required after assembly, apart from adjustment of RV1, a side-adjustable preset potentiometer. Board 1 was fully accessible to enable the four DIL switches to be operated. The slightly smaller size of board 1 was to aid soldering to the Veropins along one edge of board 2.

A number of arrangements of the controls on the diecast box is possible. The arrangement used in the prototype can be surmised from the photograph. A battery holder and cable to the transceiver were fixed to one end, two 3.5mm audio jacks and two toggle switches were fitted to the opposite end. On the base of the box were five push-button switches for triggering the messages, an electret microphone for making recordings, an *Overflow* LED and a group of holes to allow a small internal loudspeaker to be heard.

The Veroboard layouts for the two PCBs are shown in **Fig 4** and **Fig 5**. As the unit was constructed mainly using junk box components, 3.75in-wide Veroboard was used. This width appears to have been superseded by 100mm-wide material, available from Maplin as a 100mm-long piece under code JP49D. If the old size board is to be used, it will be necessary to drill five 1mm holes in the undrilled border track for D35 etc at the bottom of board 1, see Fig 4.

For R13, a 7 x 47kΩ single-in-line (SIL) resistor array is used which has seven 47kΩ resistors, all connected to a common pin at one end, usually marked with a dot. If one of these is not available, the more common eight-resistor version (Maplin RA31J) can be utilised with the appropriate end pin removed. Alternatively, use separate resistors. ♦

REFERENCE

[1] ISD Chipcorder Data Book. Information Storage Devices, Inc, 2045 Hamilton Avenue, San José, California 95125, USA. www.isd.com tel: 408-369-2400. UK agents: Sequoia Technology Ltd, Tekelec House, Back Lane, Spencers Wood, Reading, Berks RG7 1PW, tel: 0118 925 8000.

PROGRAMMING

FIRSTLY, DECIDE ROUGHLY what your announcements are going to be, and determine the duration of each, rounded up to the next 1.6 second step. Set the DIL switches S6 to S9 accordingly.

As an example, assume message 1 is going to be 20 seconds long. The first message always starts at time zero seconds. Message 2 can therefore start at time 20.8 seconds, the next multiple of 1.6 seconds. Using Table 1 set S6 to 20.8 seconds. Assume message 2 will be 10 seconds long, taking us to 30.8 seconds. The next step after 30.8 is 32 so set S7 to 32 seconds. Continue and set S8 and S9 similarly.

After setting the DIL switches, the recordings can be made. Find a quiet location. Put S11 in the *Record* position. Press and hold S1 while speaking clearly into the electret microphone, keeping an eye on the seconds hand of your watch. Release S1 when you have finished speaking, hopefully before the time you have chosen for your next recording to start. Recording will continue *for as long as you press S1*, even if you overrun into the next recording period. You can play back your recording straight away by putting S11 in the *Playback* position and momentarily pressing S1.

To record message 2, put S11 in the *Record* position, then press and hold S2 while talking into the microphone. To play back, put S11 in the *Playback* position and momentarily press S2.

The remaining messages can be recorded in a similar manner.

DIL switch / Step (s)	a 1.6	b 3.2	c 6.4	d 12.8	e 25.6	f 51.2
Time (s)						
0.0	C	C	C	C	C	C
1.6	O	C	C	C	C	C
3.2	C	O	C	C	C	C
4.8	O	O	C	C	C	C
6.4	C	C	O	C	C	C
8.0	O	C	O	C	C	C
9.6	C	O	O	C	C	C
11.2	O	O	O	C	C	C
12.8	C	C	C	O	C	C
14.4	O	C	C	O	C	C
16.0	C	O	C	O	C	C
17.6	O	O	C	O	C	C
19.2	C	C	O	O	C	C
20.8	O	C	O	O	C	C
22.4	C	O	O	O	C	C
24.0	O	O	O	O	C	C
25.6	C	C	C	C	O	C
27.2	O	C	C	C	O	C
28.8	C	O	C	C	O	C
30.4	O	O	C	C	O	C
32.0	C	C	O	C	O	C
33.6	O	C	O	C	O	C
35.2	C	O	O	C	O	C
36.8	O	O	O	C	O	C
38.4	C	C	C	O	O	C
40.0	O	C	C	O	O	C
41.6	C	O	C	O	O	C
43.2	O	O	C	O	O	C
44.8	C	C	O	O	O	C
46.4	O	C	O	O	O	C
48.0	C	O	O	O	O	C
49.6	O	O	O	O	O	C
51.2	C	C	C	C	C	O
52.8	O	C	C	C	C	O
54.4	C	O	C	C	C	O
56.0	O	O	C	C	C	O
57.6	C	C	O	C	C	O
59.2	O	C	O	C	C	O
O - switch open				C - switch closed		

Table 1: Setting the DIL switches S6 - S9.

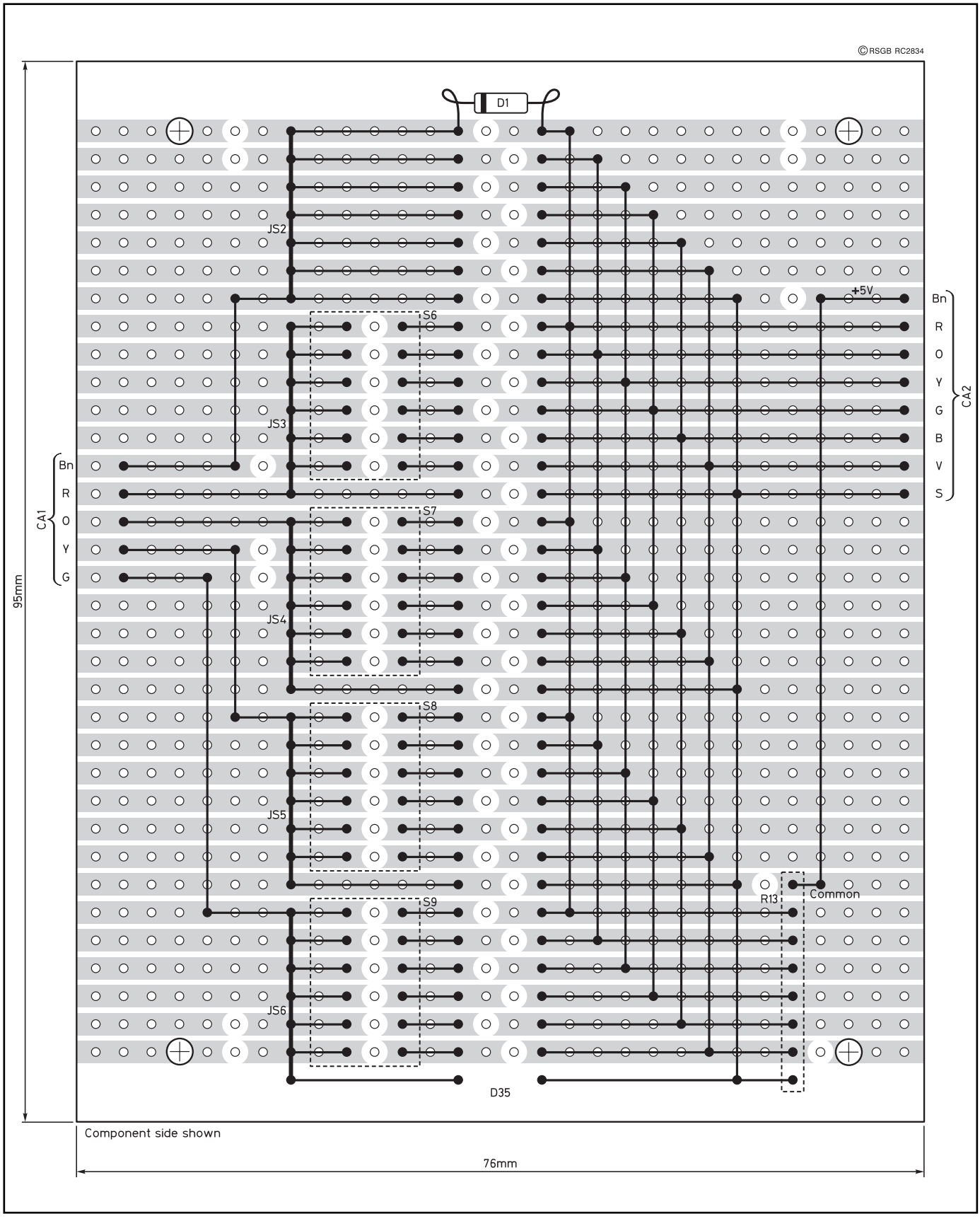


Fig 4: Layout of board 1.

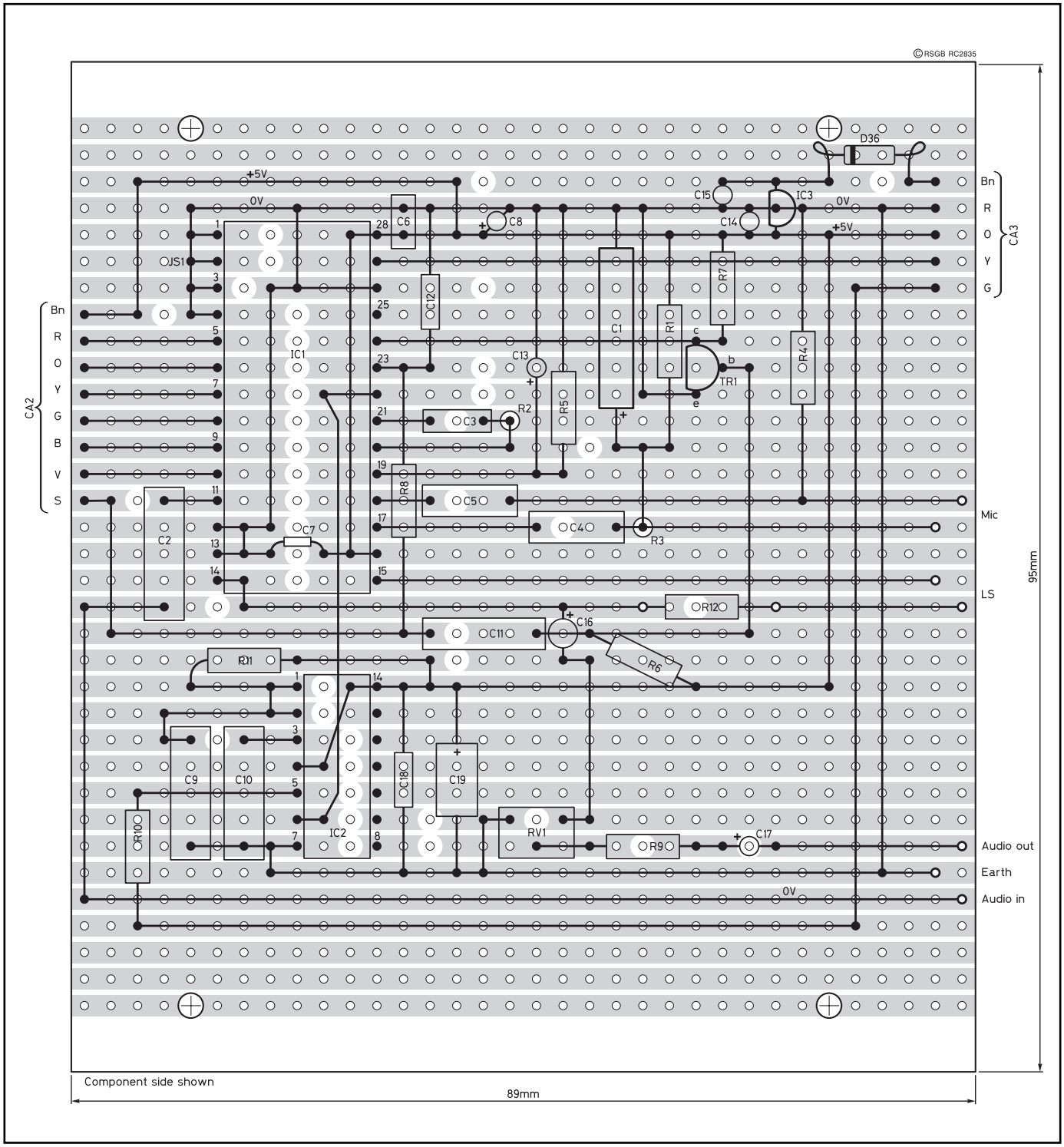


Fig 5: Layout of board 2.